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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,753	WIDIGEN, LARRY	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001 and 03 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Drawings as received on 7/03/2001 and IDS as received on 7/03/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The present title, "Method and Apparatus for Dynamic Register Management in a Processor" is generic and relates to any method of managing registers rather than the specific method presented in the claim language. Please amend the title to be more descriptive of the function of the invention as claimed.

6. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means"

and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

7. The abstract contains language such as "generally" which make it unclear whether the features described after the language are part of the invention or not.

8. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and **should include that which is new in the art to which the invention pertains**. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

9. The abstract does not disclose much of the subject matter presented in the claim language. Furthermore, the information the abstract does disclose is well known in the art and does not provide any insight into the actual disclosure of the invention. Please amend the abstract to more distinctly point out the features of the invention.

Claim Objections

10. Claims 1, 3, 11-14 and 19 are objected to because of the following informalities:

a. Claim 1 recites the language, "a status indicator for indicating the status of each virtual register" on p.38. Please change this to read, "a status indicator for indicating **a** status of each virtual register" so as to provide the correct antecedent basis for the limitation "the status".

b. Claim 3 recites the language, "setting to clean at least status of the virtual register" on lines 20-21 of p.38. It is unclear what is meant by the "at least status." However, the Examiner assumes that this is a typographical error, and requests that the language be changed to read similarly to, "setting to clean the status of the virtual register." Furthermore, for the purposes of this examination, the Examiner will assume that the above requested change is how the claim language is to be interpreted.

c. Claim 11 recites the limitation, "wherein the binding comprises" on line 29 of p.39. It is unclear whether "the binding" refers to the method steps claimed in claim 10, or whether it is a separate step that is unrelated, and thus lacks antecedent basis. Please correct the claim language to more clearly point out what "the binding" refers to. See also similar language in claims 12-14.

d. Claim 14 recites the limitation, "wherein subsequent the binding when the first virtual register is a destination register." This is not correct idiomatic English. Please correct the claim language to read more similarly to, "wherein following

the binding, if the first virtual register is a destination register" so that it is clear what is meant by the claim language.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 5, 7, 9 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Regarding claim 5, the language, "A comparator, which detects the value in each of the status bits of the plurality of status bits, wherein the values in the status bits associated with the saving of a status on a stack is accomplished by saving a value in at least one status bit on the stack" is recited on line 1 of p.39. This sentence is not correct idiomatic English. It is unclear how the comparator relates to the saving of a status on a stack, if it relates at all. It is also unclear what "the values in the status bits....is accomplished" means, as the incorrect language makes it impossible to determine what is meant from this sentence. For the purposes of this examination, the Examiner will assume that the language is meant to convey a comparator, which detects the value in each of the status bits of the plurality of status bits, as well as the limitation that at least one value of a status bit is saved on the stack. See also similar language in claim 19.

14. Regarding claim 7, the language, "The method.... further comprising executing a save command, comprising:" is recited on lines 9-10 of p.39. It is unclear whether the second "comprising" limitation refers to the method of the parent claim, or to the execution of a save command. Please correct the claim language to more distinctly point out what this limitation is in reference to.

15. Regarding claim 9, the language, "The method.... further comprising executing a restore command, comprising:" is recited on lines 18-19 of p.39. It is unclear whether the second "comprising" limitation refers to the method of the parent claim, or to the execution of a restore command. Please correct the claim language to more distinctly point out what this limitation is in reference to.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

17. Claims 1 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al., U.S. Patent No. 6,298,435.

18. Regarding claim 1, Chan has taught a method of mapping a plurality of virtual registers to a plurality of physical registers comprising:

a. Providing a plurality of virtual registers, wherein each virtual register comprises physical register address bits (see Col.4 lines 20-33),

b. Providing a status indicator for indicating the status of each virtual register (see Col.5 lines 5-16).

19. Regarding claim 15, Chan has taught the method of claim 1, wherein the status indicator comprises:

a. A plurality of status bits, wherein each virtual register of the plurality of virtual registers is associated with at least one of the status bits of the plurality of status bits (see Col.5 lines 5-16),

b. A comparator, which detects the value in each of the status bits of the plurality of status bits. While not taught explicitly, there is inherently some sort of comparator which recognizes the values of the status bits, allowing the processor to determine the states of the virtual registers so they can be read/written appropriately, as well as because not having something to create meaning of the values in the status bits would make having the status bits worthless.

20. Regarding claim 16, Chan has taught a processing device, comprising:

a. A plurality of physical registers (see Col.4 lines 20-33),

b. A plurality of virtual registers, wherein each virtual register comprises physical register address bits (see Col.4 lines 20-33),

c. A status indicator for indicating a status of each virtual register (see Col.5 lines 5-16).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 2-9 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al., U.S. Patent No. 6,298,435 as applied to claims 1 and 6, respectively, above, and further in view of Yeager et al., U.S. Patent No. 5,758,112.

23. Regarding claim 2, Chan has taught the method as recited in claim 1, but has not explicitly taught where the method further comprises:

a. Mapping a virtual register from an old physical register to a new physical register, when the virtual register is a destination virtual register of an instruction being decoded,

b. Placing an address of the old physical register in an instruction retirement list related to the instruction being decoded if an only if the status indicator indicates that the virtual register is not clean.

24. However, Yeager has taught the updated mapping of logical registers to new physical registers after every instruction is decoded (see Col.6 lines 41-45), and the saving of the old physical register, if it has been written to (i.e. not clean) (see Col.7 line 64 – Col.8 line 6), to an active list so that it can be restored later if needed (see Col.6 lines 45-50 and Col.7 lines 54-63). One of ordinary skill in the art would have recognized that it is desirable to increase processing speed in a microprocessor, while keeping complexity to a minimum. Renaming in this manner

simplifies dependency checking by making it unambiguous and increases processing speed by reducing the penalty associated with branch mispredictions or exceptions (see Col.6 lines 45-60). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chan to place the address an old physical register on an active list when its associated logical register is mapped to a new register and is not clean as taught by Yeager, so that the speed of the microprocessor is increased and the complexity of dependency checking decreased.

25. Regarding claim 3, Chan in view of Yeager has taught the method as recited in claim 2, further comprising saving a physical register address held in a virtual register to a stack (see Yeager Col.17 lines 26-38).

26. Chan in view of Yeager has not explicitly taught saving a status of the virtual register indicated by the status indicator to a stack and setting to clean at least status of the virtual register.

27. However, Chan has taught the use of status indicators to show if a virtual register is valid and has been written into or not (see Chan Col.5 lines 5-16). One of ordinary skill in the art would have recognized that in order to restore a "precise state" as necessitated by Yeager (see Yeager Col.17 lines 26-38), one would have to know which parts of the state were valid and which were not. Furthermore, because the saving of the local virtual registers onto the stack records the changes made to the local virtual registers (see Yeager Col.17 lines 35-38), one would have recognized that the status indicators of Chan would have been updated to reflect the new assignments and writes, as that is the purpose of the indicators (see Chan Col.5 lines 5-16). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chan in view of Yeager to include saving the virtual register status indicators on the stack when

saving the local virtual registers so that a correctly precise state can be restored from the stored information.

28. Furthermore, one of ordinary skill in the art would have recognized that in a context switch, such as in the execution of a branch instruction (see Yeager Col.17 lines 26-38), there is no purpose to preserving the state of the registers if they are not going to be overwritten in the new state and thus necessitating a restore of the previous state. Therefore, because the status indicators of the virtual registers dictate whether data new data can be written to them without overwriting valid data (see Chan Col.5 lines 5-16), one of ordinary skill in the art would have found it obvious to set the status indicators to "clean" after executing a context switch so that the new registers are able to be written to and thus justifying the preservation of their previous values.

29. Regarding claim 4, Chan in view of Yeager has taught the method as recited in claim 2, but has not explicitly taught wherein the method further comprises setting the status of a virtual register to not clean when the virtual register is mapped to a new physical register.

30. However, Chan in view of Yeager has taught the mapping of a virtual register to a new physical register when it has a status of not clean (see above paragraph 24). One of ordinary skill in the art would have recognized that this updating of the mapping does not affect the status of the virtual register as other instructions may still be pointing to it, but rather only affects where the data that is mapped with that virtual register is stored. Furthermore, changing the status of the virtual register could prevent the register from being saved or restored during a context switch, producing incorrect results. Therefore one of ordinary skill in the art would have

found it obvious to set the status of the virtual register having an updated mapping to "not clean" so that the status of the virtual register remains unchanged, and undesirable results are avoided.

31. Regarding claim 5, Chan in view of Yeager has taught the method as recited in claim 4, wherein the status indicator comprises:

a. A plurality of status bits, wherein each virtual register of the plurality of virtual registers is associated with at least one of the status bits of the plurality of status bits (see Col.5 lines 5-16),

b. A comparator, which detects the value in each of the status bits of the plurality of status bits, wherein the values in the status bits associated with the saving of a status on a stack is accomplished by saving a value in at least one status bit on the stack (see paragraphs 27-28).

32. While not taught explicitly, there is inherently some sort of comparator that recognizes the values of the status bits and creates meaning from them, allowing the processor to determine the states of the virtual registers so they can be read/written appropriately. Without such a comparator, there would be nothing to create meaning of the values in the status bits, thus making having the status bits worthless.

33. Regarding claim 6, Chan has taught the method as recited in claim 1, but has not explicitly taught the method further comprising designating a plurality of virtual registers of the plurality of virtual registers as virtual local registers.

34. However, Yeager has taught that a subset of the virtual registers which reside in the mapping tables are saved on the branch stack so that a precise restore point for a branch instruction can be restored (see Col.17 lines 26-38). Here, the logical destination registers of the

possible branch instructions are saved, which can be considered "local" to each branch instruction. Because it is necessary to restore a precise state upon return from a branch instruction rather than an imprecise state so that processing results are correct, one of ordinary skill in the art would have found it obvious to modify the processor of Chan to designate a plurality of the virtual registers as "local" so that the registers can be used to save and restore the state of branch instructions on a branch stack.

35. Regarding claim 7, Chan in view of Yeager has taught the method as recited in claim 6, further comprising executing a save command, comprising:

a. Saving the mapping of all virtual local registers onto a stack (see Yeager Col.17 lines 26-38),

36. Chan in view of Yeager has not explicitly taught the saving a status as indicated by the status indicator for each of the virtual local registers onto the stack. However, Chan has taught the use of status indicators to show if a virtual register is valid and has been written into or not (see Chan Col.5 lines 5-16). One of ordinary skill in the art would have recognized that in order to restore a "precise state" as necessitated by Yeager (see Yeager Col.17 lines 26-38), one would have to know which parts of the state were valid and which were not. Furthermore, because the saving of the local virtual registers onto the stack records the changes made to the local virtual registers (see Yeager Col.17 lines 35-38), one would have recognized that the status indicators of Chan would have been updated to reflect the new assignments and writes, as that is the purpose of the indicators (see Chan Col.5 lines 5-16). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chan in view of Yeager to include saving the

virtual register status indicators on the stack when saving the local virtual registers so that a correctly precise state can be restored from the stored information.

37. Regarding claim 8, Chan in view of Yeager has taught the method as recited in claim 7, but has not explicitly taught wherein the save command further comprises setting the status of all virtual local registers to "clean".

38. However, one of ordinary skill in the art would have recognized that in a context switch, such as in the execution of a branch instruction (see Yeager Col.17 lines 26-38), there is no purpose to preserving the state of the registers if they are not going to be overwritten in the new state and thus necessitating a restore of the previous state. Therefore, because the status indicators of the virtual registers dictate whether data new data can be written to them without overwriting valid data (see Chan Col.5 lines 5-16), one of ordinary skill in the art would have found it obvious to set the status indicators to "clean" after executing a context switch so that the new registers are able to be written to and thus justifying the preservation of their previous values.

39. Regarding claim 9, Chan in view of Yeager has taught the method as recited in claim 8, further comprising executing a restore command, comprising:

a. Popping the mapping of all virtual local registers from the stack to the virtual local registers (see Col.17 lines 5-13, 26-38).

40. Chan in view of Yeager has not explicitly taught wherein executing a restore command further comprises:

b. Popping the status of all virtual local registers from the stack.

41. However, Official Notice is taken that a stack generally functions as temporary storage, with data being pushed on to it to temporarily save it, and later popped off to restore a previous state. Therefore, because Chan in view of Yeager has taught the pushing of the mapping of local virtual registers along with their corresponding statuses (see paragraphs 27-28 above), it would have been obvious to one of ordinary skill in the art to pop the statuses corresponding to the local virtual registers so that a previous state could be fully restored.

42. Regarding claim 17, Chan has taught the processing device as recited in claim 16, further comprising:

a. An instruction decoder for decoding an instruction (109 of Fig.1).

43. Chan has not explicitly taught the following:

b. An instruction retirement list,

c. Machine-readable code for mapping a virtual register from an old physical register to a new physical register, when the virtual register is a destination virtual register of an instruction being decoded,

d. Machine-readable code for placing an address of the old physical register in an instruction retirement list related to the instruction being decoded if an only if the status indicator indicates that the virtual register is not clean.

44. However, Yeager has taught the updated mapping of logical registers to new physical registers after every instruction is decoded (see Col.6 lines 41-45), and the saving of the old physical register, if it has been written to (i.e. not clean) (see Col.7 line 64 – Col.8 line 6), to an active list so that it can be restored later if needed (see Col.6 lines 45-50 and Col.7 lines 54-63). One of ordinary skill in the art would have recognized that it is desirable to increase processing

speed in a microprocessor, while keeping complexity to a minimum. Renaming in this manner simplifies dependency checking by making it unambiguous and increases processing speed by reducing the penalty associated with branch mispredictions or exceptions (see Col.6 lines 45-60). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chan to place the address an old physical register on an active list when its associated logical register is mapped to a new register and is not clean as taught by Yeager, so that the speed of the microprocessor is increased and the complexity of dependency checking decreased.

45. Regarding claim 18, Chan in view of Yeager has taught the processing device as recited in claim 17, further comprising a stack, wherein a physical register address held in a virtual register is saved to the stack.

46. Chan in view of Yeager has not explicitly taught wherein one status bit associated with the virtual register of the plurality of virtual registers is saved to the stack and the status of the saved virtual register is set to clean.

47. However, Chan has taught the use of status indicators to show if a virtual register is valid and has been written into or not (see Chan Col.5 lines 5-16). One of ordinary skill in the art would have recognized that in order to restore a "precise state" as necessitated by Yeager (see Yeager Col.17 lines 26-38), one would have to know which parts of the state were valid and which were not. Furthermore, because the saving of the local virtual registers onto the stack records the changes made to the local virtual registers (see Yeager Col.17 lines 35-38), one would have recognized that the status indicators of Chan would have been updated to reflect the new assignments and writes, as that is the purpose of the indicators (see Chan Col.5 lines 5-16). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of

Chan in view of Yeager to include saving the virtual register status indicators on the stack when saving the local virtual registers so that a correctly precise state can be restored from the stored information.

48. Furthermore, one of ordinary skill in the art would have recognized that in a context switch, such as in the execution of a branch instruction (see Yeager Col.17 lines 26-38), there is no purpose to preserving the state of the registers if they are not going to be overwritten in the new state and thus necessitating a restore of the previous state. Therefore, because the status indicators of the virtual registers dictate whether data new data can be written to them without overwriting valid data (see Chan Col.5 lines 5-16), one of ordinary skill in the art would have found it obvious to set the status indicators to "clean" after executing a context switch so that the new registers are able to be written to and thus justifying the preservation of their previous values.

49. Regarding claim 19, Chan in view of Yeager has taught the processing device, as recited in claim 18, wherein the status indicator comprises:

a. A plurality of status bits, wherein each virtual register of the plurality of virtual registers is associated with at least one of the status bits of the plurality of status bits (see Col.5 lines 5-16),

b. A comparator, which detects the value in each of the status bits of the plurality of status bits, wherein the values in the status bits associated with the saving of a status on a stack is accomplished by saving a value in at least one status bit on the stack (see paragraphs 27-28).

50. While not taught explicitly, there is inherently some sort of comparator that recognizes the values of the status bits and creates meaning from them, allowing the processor to determine the states of the virtual registers so they can be read/written appropriately. Without such a comparator, there would be nothing to create meaning of the values in the status bits, thus making having the status bits worthless.

51. Regarding claim 20, Chan in view of Yeager has taught the processing device as recited in claim 19, but has not explicitly taught wherein the status of a virtual register is set to not clean when the virtual register is mapped to a new physical register.

52. However, Chan in view of Yeager has taught the mapping of a virtual register to a new physical register when it has a status of not clean (see above paragraph 24). One of ordinary skill in the art would have recognized that this updating of the mapping does not affect the status of the virtual register as other instructions may still be pointing to it, but rather only affects where the data that is mapped with that virtual register is stored. Furthermore, changing the status of the virtual register could prevent the register from being saved or restored during a context switch, producing incorrect results. Therefore one of ordinary skill in the art would have found it obvious to set the status of the virtual register having an updated mapping to "not clean" so that the status of the virtual register remains unchanged, and undesirable results are avoided.

53. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al., U.S. Patent No. 6,298,435 in view of Yeager et al., U.S. Patent No. 5,758,112 as applied to claims 2-9 and 17-20 above, and further in view of Yung et al., U.S. Patent No. 5,546,554.

54. Regarding claim 10, Chan in view of Yeager has taught the method as recited in claim 9 above, but has not explicitly taught wherein the method further comprises:

a. Binding a first virtual register of the plurality of virtual registers to a second virtual register of the plurality of virtual registers.

b. Binding the status of the first virtual register to a second virtual register.

55. However, Yung has taught when a virtual register is a destination register of an instruction, a new mapping for the virtual register is created so that the original physical register corresponding to the original virtual register is not overwritten, effectively creating a new virtual register that is identical to the original virtual register except that it is mapped to a new physical register (see Col.8 lines 10-40). Because having data overwritten can cause incorrect processing results which are unacceptable in a processor, one of ordinary skill in the art would have found it obvious to modify the process taught by Chan in view of Yeager to create a new mapping for a virtual register when it is the destination of an instruction, so that data in the physical register of the original mapping is not overwritten, thus avoiding potential incorrect results.

56. Furthermore, Chan in view of Yeager has taught the association of status indicators with virtual registers, and their subsequent storage when the virtual registers are saved during context switches because everything associated with that register needs to be saved to restore the precise state (see above paragraphs 27-28). One of ordinary skill in the art would have recognized that because Yung is creating a new mapping to be an identical virtual register to an original so it appears the same to the instruction, everything associated with the register needs to be mirrored in the new virtual register so that it is the same in everyway. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chan in view of Yeager with the teachings of Yung so that when binding a virtual register to a new virtual register the associated

status is bound also so that a precise copy is created, allowing a precise state to be restored if needed.

57. Regarding claim 11, Chan in view of Yeager in further view of Yung has taught the method as recited in claim 10, wherein the binding comprises placing a physical address stored in the second virtual register in the first virtual register and setting the status of the first virtual register to the status of the second virtual register (see Yung Col.8 lines 10-40, as well as above paragraphs 46-47).

58. Regarding claim 12, Chan in view of Yeager in further view of Yung has taught the method as recited in claim 11, wherein the binding further comprises:

a. Saving the mapping of the first virtual register onto the stack cache (see Yeager Col.17 lines 26-38),

b. Saving the status of the first virtual local register onto the stack cache (see above paragraph 27-28).

59. Regarding claim 13, Chan in view of Yeager in further view of Yung has taught the method as recited in claim 12, wherein the binding occurs during a call instruction, wherein the call instruction has at least one argument, wherein the first virtual register is used for the at least one argument. Here, a branch instruction can be considered a "call" instruction in that it executes code at a new location, and requires that an operand be supplied, generally via a register, to provide an offset. Because Chan in view of Yeager in view of Yung has taught that the binding operation involves saving virtual registers to the stack in response to a branch instruction (see paragraphs 55-56 above and Yeager Col.6 lines 35-60), one of ordinary skill in the art would have found it obvious to consider a branch instruction as a call instruction.

60. Regarding claim 14, Chan in view of Yeager in further view of Yung has taught the method of claim 14 as recited in claim 11, wherein subsequent the binding when the first virtual register is a destination register, the first virtual register is assigned a physical register address which is different than a physical register address stored in the second virtual register (see Yung Col.8 lines 10-40). Here, it is inherent that the new physical address is different than the original physical address as otherwise the data in the original would be overwritten, which is what Yung is avoiding.

Conclusion

61. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

62. Witt, U.S. Patent No. 6,122,656, has taught a processor which implements register renaming using virtual registers mapped to physical registers, as well as saving and restoring a processor state upon an exception occurring.

63. Clift et al., U.S. Patent No. 5,727,176, has taught a processor that implements register renaming using logical registers mapped to physical registers, as well as implementing a retirement list that maintains register values of non-speculative operations.

64. Farrell et al., U.S. Patent No. 6,405,304, has taught a method for register renaming which includes the ability to restore a state of the registers from a copy placed in vector memory.

65. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

66. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
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BJO
2/18/2004

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